AMENDMENTS TO THE SPECIFICATION

Please amend the title in all instances as follows:

~~DRIVER WITH BULK SWITCHING~~ MOS ~~POWER~~ TRANSISTOR WITH SERRATED GATE STRUCTURES

Please insert the following paragraph as the first paragraph on page 1:

This is a divisional application of Application Serial No. 10/272,035 filed on October 15, 2002.

Please amend the second paragraph on page 1 to read:

A MOS transistor is a well-known circuit device that controllably varies the current that flows between a source region and a drain region. A MOS power transistor is a larger MOS transistor that is capable of handling much larger magnitudes of current. A driver is another ~~well-know~~ well-known circuit device that utilizes a PMOS power transistor and an NMOS power transistor.

Please amend the last paragraph on page 5 (which continues over to page 6) to read:

FIGs. 2A-2B show timing diagrams that ~~illustrates~~ illustrate the operation of gate signal generator 110 in accordance with the present invention. As shown in FIGs. 2A-2B, gate signal generator 110 outputs the gate signals G1 and G2 so that the voltage on gate signal G2 is equal to or less than a turn off voltage TF1 (that turns off transistor M5) before the voltage on gate signal G1 is equal to a turn on voltage TN1 (that turns on transistor M0). Similarly, the voltage on gate signal G1 is equal to or greater than a turn off voltage TF2 (that turns off transistor M0) before

the voltage on gate signal G2 is equal to a turn on voltage TN2 (that turns on transistor M5).

Please amend the third paragraph on page 6 to read:

FIG. 3 shows a circuit diagram that illustrates an example of a gate signal generator 300 in accordance with the present invention. As shown in FIG. 3, gate signal generator 300 has a p-channel delay path 310 that includes a p-path inverter 312, and an n-channel delay path 314 that includes ~~a~~ an n-path inverter 316.

Please amend the second paragraph on page 7 to read:

N-path inverter 316 includes a PMOS transistor M18 and ~~a~~ an NMOS transistor M15 that have gates connected to a gate node NG2 and drains that are connected to the gate of transistor M5. Further, as shown in FIG. 3, n-path 314 can include additional inverters that are connected in series.

Please amend the last paragraph on page 7 (which continues onto page 8) to read:

Returning again to FIG. 1, driver stage 100 additionally includes a first switch SW1 that is connected to ~~ground VSS,~~ the control signal CS, and the well of transistor M0 via node N2; and a second switch SW2 that is connected to ground VSS and the control signal CS. In addition, driver stage 100 includes a resistor R46 that is connected to the well of transistor M0 via node N2 and to switch SW2.

Please amend the second paragraph on page 8 to read:

As shown in FIG. 4B, switch SW2 can be implemented as ~~a~~ an n-channel MOS transistor M27 that has an n+ source connected to ground VSS and an n+ drain

connected to resistor R. In addition, transistor M27 has a gate connected to the control signal CS, and a substrate connected to a p bulk voltage PBULK.